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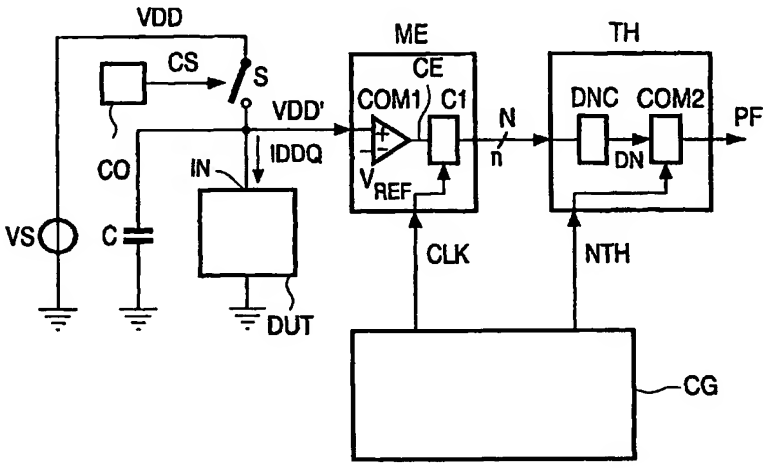
(54) Title: METHOD AND APPARATUS FOR DETERMINING IDDQ



(57) Abstract: A test apparatus for testing a device under test (DUT) to detect a defect comprises a measurement circuit (ME), a threshold circuit (TH), and a control circuit (CG). The measurement circuit (ME) comprises a counter (C1) which counts clock pulses (CLK) during a count period (TC) to obtain a counted number (N) of clock pulses (CLK). The count period (TC) has a start determined by the start (t1) of a testing cycle which occurs at the instant a switch (S) which is coupled to an terminal (IN) of the device under test (DUT) removes a power supply voltage (VDD) from the terminal (IN) and the voltage (VDD') at the terminal (IN) starts decaying. An end of the count period (TC) is determined by an instant (t2) a comparator (COM1) detects that the voltage (VDD') at the terminal (IN) crosses a reference value (VREF). The control circuit (CG) generates the clock signal (CLK) and/or a reference number (NTH) taking into account the variability of the manufacturing process of the circuit under test (CUT). The threshold circuit (TH) generates a pass/fail signal (PF) by comparing the counted number (N) and the reference number (NTH).

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